REMARKS

Applicants respectfully traverse and request reconsideration.

Applicants wish to thank the Examiner for the notice that claims 8, 9, 12, 13 and 16 would be allowed if rewritten in independent form. Applicants also wish to thank the Examiner for the notice that claims 20-27 are allowed.

Claims 7, 10, 11, 14 and 17 stand rejected under 35 U.S.C. §103(a) as being unpatentable over So in view of Watts. All of the claims were previously in condition for allowance, but the Office has issued a new office action, and these are new grounds of rejection. Applicants respectfully submit the cited references do not teach what is alleged and therefore the claims are again in condition for allowance. The So reference is directed to an integrated circuit that provides a single chip for use with a first processor that is off-chip, and terminals for a first processor's related signals that define a first data width, additional terminals for external bus related signals (PCI) and third terminals for memory related signals, and a DRAM memory controller connected to the third terminals. The So reference describes a conventional prior art implementation employing a separate CPU integrated circuit, separate Northbridge circuit, separate Southbridge circuit and other integrated circuits that were conventional at the time. Such systems were generally described in Applicants' "Background of the Invention" section. So, like other prior art solutions, require for example, an off-chip interfacing bus, corresponding drivers and receivers and additional pin count on the separate integrated circuits and lack structure and advantages of Applicants' claimed integrated personal computing system.

So does not contemplate or describe in the cited portions, any central processing unit on the same substrate as a Northbridge, which also contains a bus on the substrate that is operably coupled between the central processing unit and a Northbridge on the substrate as claimed. The office action states that So teaches "wherein the Northbridge is contained on the substrate [that

also contains the CPU] (see integrated circuits in column 2, lines 4-8 for background, see also ASIC in column 16, lines 29-35, see also processors and bus suitably fabbed on the single chip in column 15, line 32)" (page 3 of office action). However, Applicants respectfully submit that each of these sections do not teach what is alleged. For example, the portion of column 2, lines 4-8 make no mention whatsoever of any Northbridge and CPU being contained on the same substrate. In fact, So describes an opposite system from that claimed. For example, the ASICs referred to in column 16, lines 29-35 are actually separate integrated circuits that are connected to a CPU via a PCI bus. This is a conventional architecture for example, shown in Applicants' FIG. 1 (prior art figure). In addition, the Abstract of So also states that the integrated circuit 320 is for use with another off-chip processor 106 with interconnections with an external PCI bus. Applicants claim a different structure and Applicants respectfully submit that the So reference does not teach what is alleged and therefore, the claims are in condition for allowance.

In addition, the claim requires, among other things, that the memory access request from the central processing unit is done at an operating rate of the processing unit wherein the memory controller receives memory access request from the memory access request buffer. The office action cites column 39, lines 13-60 as allegedly teaching this subject matter, however no such teaching can be found. The teaching actually refers to a DSP, not a CPU and a PCI bus. A PCI bus as known in the art does not operate at an operating rate of a central processing unit. Other differences will be recognized by those of ordinary skill in the art.

Applicants also respectfully traverse the rejection with respect to the Watts reference and respectfully submit that because the So reference does not teach what is alleged, that the combination of So and Watts also do not teach the claimed subject matter. Other differences with respect to the Watts reference will also be recognized by those of ordinary skill in the art.

Applicants respectfully submit that the claims are in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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